REMARKS

This paper is responsive to a Non-Final Office Action dated November 2, 2004. Claims 1-25 were examined. Claims 1-14, 17, and 19-23 are objected to for informalities. Claims 1-14 stand rejected under 35 U.S.C. § 112, second paragraph. Claims 1-4, 6, 7, 11, 15-17, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,542,040 to Lesea in view of Applicants' Admitted Prior Art. Claims 10, 12, 18, 19, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lesea in view of Applicants' Admitted Prior Art and U.S. Patent No. 6,178,212 to Akashi. Claims 5 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lesea in view of Applicants' Admitted Prior Art and U.S. Patent No. 5,036,298 to Bulzachelli. Claims 8, 9, and 20-23 are indicated as including allowable subject matter.

Amendments to the Specification

The specification is amended to include provisional priority data as referred to on the Application Data Sheet filed June 25, 2001. No new matter is added. Note that the reference in the Application Data Sheet alone satisfies the requirements of 37 C.F.R. § 1.78(a)(5)(iii).

Amendments to the Drawings

Figures 1A, 1B, 1C, 2, and 3 are amended to include the legend "PRIOR ART." No new matter is added.

Claim Objections

Claims 1-14, 17, and 19-23 are objected to for informalities. Claims 7, 8, 20, and 22 are amended to provide antecedent basis. Claims 8, 9, and 17 are amended to correct typographical errors. Applicants believe that the original claims 1 and 13 are in proper form and claims 7, 8, 9, 17, 19, 20, and 22 are in proper form as amended. Claims 2-6, 10-12, 14, 21, and 23 depend directly or indirectly from original claim 1, amended claim 20, or amended claim 22, claims believed to be in proper form. Accordingly, Applicants respectfully request that the objections to claims 1-14, 17, and 19-23 be withdrawn.

Claim Rejections Under 35 U.S.C. § 112

Claims 1-14 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Referring to claim 1, the Office Action states that "lines 2, 8, and 10, respectively, recite '...coupled to...'. However, it is unclear and indefinite as to which element is coupled to." In claim 1, the language "...coupled to..." is synonymous with "...configured to..." Applicants respectfully maintain that the functional language of claim 1 ("...coupled to generate..." and "...coupled to receive...") serves to set definite boundaries on the patent protection sought for the claimed clock recovery circuit, and thus complies with 35 U.S.C. § 112, second paragraph. See MPEP § 2173.05(g).

Referring to claims 2 and 3, lines 2 and 2, respectively, which apparently is referring to claims 2 and 4, lines 2 and 2, respectively, the Office Action states that these lines "recite '...coupled to...'. However, it is unclear and indefinite as to which element is coupled to." In claims 2 and 4, the language "...coupled to..." is synonymous with "...configured to..." Applicants respectfully maintain that the functional language of claims 2 and 4 ("...coupled to receive...and supply..." and "...coupled to receive...and generate...," respectively) serves to set definite boundaries on the patent protection sought for the claimed clock recovery circuit, and thus complies with 35 U.S.C. § 112, second paragraph. See MPEP § 2173.05(g).

Referring to claim 8, lines 3, 4, and 9, the Office Action states that these lines "recite '...coupled to...'. However, it is unclear and indefinite as to which element is coupled to." In claim 8, the language "...coupled to..." is synonymous with "...configured to..." Applicants respectfully maintain that the functional language of claim 8 ("...coupled to receive...further coupled to receive...coupled to the output clock signal and to receive...") serves to set definite boundaries on the patent protection sought for the claimed clock recovery circuit, and thus complies with 35 U.S.C. § 112, second paragraph. See MPEP § 2173.05(g).

Accordingly, Applicants respectfully request that the rejection of claims 1-14 under 35 U.S.C. § 112, second paragraph be withdrawn.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-4, 6, 7, 11, 15-17, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,542,040 to Lesea in view of Applicants' Admitted Prior Art. Regarding claim 1, Applicants respectfully maintain that Lesea, alone or in combination with Applicants' Admitted Prior Art or other references of record, fails to teach or suggest

> a clock delay circuit coupled to receive a delay control signal derived from the difference signal and to receive the output clock signal, the clock delay circuit coupled to provide as the delayed clock signal the output clock signal delayed according to the delay control signal,

as recited in claim 1. The Office Action points to the programmable tapped-delay-line oscillator in FIG. 7 of Lesea to supply this teaching. The programmable tapped-delay-line oscillator of Lesea includes a ring oscillator whereby the frequency of the output signal, SOUT, "is changed by changing the number of inverters in the ring and/or by changing the supply voltage VSUP on supply voltage lead 113." (Col. 8, lines 19-34) The programmable tapped-delay-line oscillator of Lesea generates an output signal, SOUT, which is fed back into the programmable tapped-delay-line oscillator as DLIN to generate the next output signal SOUT for a next clock cycle according to SUPPLY 113. (FIG. 7) SOUT of Lesea is not delayed according to a delay control signal. The frequency of output signal, SOUT, of Lesea is divided by M to provide SOSC, which is fed to the phase detectors of Lesea. (Col. 4, lines 17-21; FIG. 2) The phase detectors of Lesea do not receive a delayed clock signal, but rather a frequency divided clock signal. Thus, Lesea, alone or in combination with other references of record, fails to teach or suggest

> a phase detector circuit coupled to generate a difference signal indicating a phase difference between an incoming data stream and a delayed clock signal,

as recited by claim 1. For at least these reasons, Applicants respectfully maintain that claim 1 distinguishes over Lesea, alone or in combination with all references of record. Accordingly,

Applicants respectfully request that the rejection of claim 1 and all claims dependent thereon, be withdrawn.

Regarding claim 3, Applicants respectfully maintain that Lesea, alone or in combination with Applicants' Admitted Prior Art or other references of record, fails to teach or suggest

> that the control signal for the oscillator circuit is used as the delay control signal,

as recited by claim 3. The Office Action points to the SUPPLY signal on supply voltage input lead 113 in FIG. 7 of Lesea to supply this teaching. "The frequency of the oscillating signal is changed by changing the number of inverters in the ring and/or by changing the supply voltage VSUP on supply voltage input lead 113." (Col. 8, lines 32-34) However, the programmable delay line 503 of Lesea includes a 4-to-1 multiplexer 510 and three non-inverting buffers 511-513, the output of multiplexer 510 being controlled by a four-bit digital value on select input leads 519. (Col. 8, lines 41-48) Programmable delay line 502 of Lesea includes a 512-to-1 multiplexer 520 and five hundred and eleven non-inverting buffers 521, the output of multiplexer 520 being controlled by a 14-bit digital value on select input leads 524. (Col. 8, lines 50-61; FIG. 7) Select input leads 524 and 519 are generated from BIN of Lesea. (FIG. 7) Nowhere does Lesea teach or suggest that BIN and VSUPPLY may be the same signal. For at least this reason, Applicants respectfully maintain that claim 3 distinguishes over Lesea, alone or in combination with all references of record. Accordingly, Applicants respectfully request that the rejection of claim 3 be withdrawn.

Regarding claim 14, Applicants respectfully maintain that Lesea, alone or in combination with Applicants' Admitted Prior Art or other references of record, fails to teach or suggest

> a closed loop response without an explicit zero,

as recited by claim 14. The Office Action admits that "Lesea in view of AAPA do not [sic] explicitly teach having the closed loop response without an explicit zero." The Office Action relies on Lesea and AAPA in combination with Bulzachelli to supply this teaching. However, the Office Action fails to provide a motivation to combine the phase-locked loop of Lesea to have the closed loop response of Bulzachelli and Applicants respectfully maintain that there is no

motivation to combine the phase-locked loop of Lesea to have the closed loop response of Bulzachelli.

> In holding an invention obvious in view of a combination of references, there must be some suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them in the way that would have produced the claimed invention.

See Karsten Mfg. Corp. v. Cleveland Golf. Co., 58 USPQ2d 1286, 1293 (Fed. Cir. 2001). Thus, Lesea alone or in combination with other references of record fails to teach or suggest the clock recovery circuit of claim 1 with a closed loop response without an explicit zero. For at least this reason, Applicants respectfully maintain that claim 14 distinguishes over Lesea, alone or in combination with all references of record. Accordingly, Applicants respectfully request that the rejection of claim 14 be withdrawn.

Regarding claim 15, Applicants respectfully maintain that Lesea, alone or in combination with Applicants' Admitted Prior Art or other references of record, fails to teach or suggest

> receiving the output clock signal in a delay circuit and generating the delayed clock signal from the output clock signal according to a delay control signal derived from the difference signal,

as recited in claim 15. The Office Action points to the programmable tapped-delay-line oscillator in FIG. 7 of Lesea to supply this teaching. The programmable tapped-delay-line oscillator of Lesea includes a ring oscillator whereby the frequency of the output signal, SOUT, "is changed by changing the number of inverters in the ring and/or by changing the supply voltage VSUP on supply voltage lead 113." (Col. 8, lines 19-34) The programmable tapped-delay-line oscillator of Lesea generates an output signal, SOUT, which is fed back into the programmable tapped-delay-line oscillator as DLIN to generate the next output signal SOUT for a next clock cycle according to SUPPLY 113. (FIG. 7) SOUT of Lesea is not delayed according to a delay control signal. The frequency of output signal, SOUT, of Lesea is divided by M to provide SOSC, which is fed to the phase detectors of Lesea. (Col. 4, lines 17-21; FIG. 2) The phase detectors of Lesea do not receive a delayed clock signal, but rather a frequency divided

clock signal. Thus, Lesea, alone or in combination with other references of record, fails to teach or suggest

> determining a phase difference between the input data stream and a delayed clock signal and generating a difference signal indicative thereof,

as recited by claim 15. For at least these reasons, Applicants respectfully maintain that claim 15 distinguishes over Lesea, alone or in combination with all references of record. Accordingly, Applicants respectfully request that the rejection of claim 15 and all claims dependent thereon, be withdrawn.

Regarding claim 24, Applicants respectfully maintain that Lesea, alone or in combination with Applicants' Admitted Prior Art or other references of record, fails to teach or suggest

> means for generating a delayed clock signal from a clock signal according to a delay control signal derived from the difference signal.

as recited in claim 24. The Office Action points to the programmable tapped-delay-line oscillator in FIG. 7 of Lesea to supply this teaching. The programmable tapped-delay-line oscillator of Lesea includes a ring oscillator whereby the frequency of the output signal, SOUT, "is changed by changing the number of inverters in the ring and/or by changing the supply voltage VSUP on supply voltage lead 113." (Col. 8, lines 19-34) The programmable tapped-delay-line oscillator of Lesea generates an output signal, SOUT, which is fed back into the programmable tapped-delay-line oscillator as DLIN to generate the next output signal SOUT for a next clock cycle according to SUPPLY 113. (FIG. 7) SOUT of Lesea is not delayed according to a delay control signal. The frequency of output signal, SOUT, of Lesea is divided by M to provide SOSC, which is fed to the phase detectors of Lesea. (Col. 4, lines 17-21; FIG. 2) The phase detectors of Lesea do not receive a delayed clock signal, but rather a frequency divided clock signal. Thus, Lesea, alone or in combination with other references of record, fails to teach or suggest

> means for detecting a phase difference between an incoming data stream and a delayed clock signal and generating a difference signal indicative thereof,

as recited by claim 24. For at least these reasons, Applicants respectfully maintain that claim 24 distinguishes over Lesea, alone or in combination with all references of record. Accordingly, Applicants respectfully request that the rejection of claim 24 and all claims dependent thereon, be withdrawn.

Claims 10, 12, 18, 19, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lesea in view of Applicants' Admitted Prior Art and U.S. Patent No. 6,178,212 to Akashi. Claims 10, 12, 18, 19, and 25 depend from claims that Applicants believe are allowable over the art of record and are allowable for at least this reason. Accordingly, Applicants respectfully request that the rejection of claims 10, 12, 18, 19, and 25 be withdrawn.

Claims 5 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lesea in view of Applicants' Admitted Prior Art and U.S. Patent No. 5,036,298 to Bulzachelli. Claims 5 and 14 depend from claims that Applicants believe are allowable over the art of record and are allowable for at least this reason. Accordingly, Applicants respectfully request that the rejection of claims 5 and 14 be withdrawn.

Allowable Subject Matter

Applicants appreciate the indication of allowable subject matter in claims 8, 9, and 20-23.

Although Applicants believe that the claims are allowable over the art of record, the reasons for allowance stated in the Office Action do not coincide with the allowed claims. Applicants do not acquiesce in additional limitations included by the reasons for allowance stated in the Office Action.

Claim 2 is amended to correct a typographical error.

Claim 4 is amended to depend from claim 1.

In summary, claims 1-25 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that, on the date shown below, this correspondence is being

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Nicole Teitler Cave — 1/26/05 (Date)

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Respectfully submitted,

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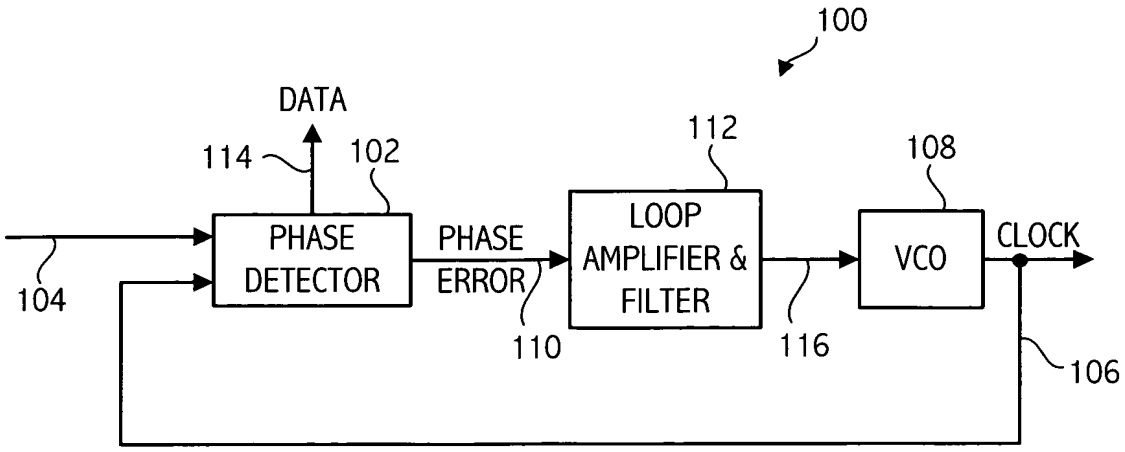
AMENDMENTS TO THE DRAWINGS

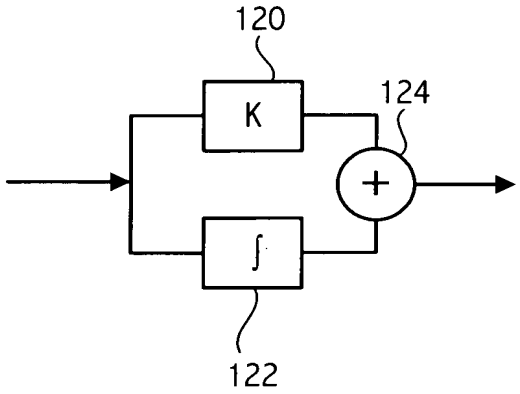
The attached sheet(s) of drawings include changes to Fig(s). 1A, 1B, 1C, 2, and 3 and replace the original sheet(s) including such figures.

Attachment(s): Replacement Sheet including amended Figs. 1A, 1B, 1C;
Replacement Sheet including amended Fig. 2;
Replacement Sheet including amended Fig. 3;
Annotated Sheet Showing Changes to amended Figs. 1A, 1B, 1C;
Annotated Sheet Showing Changes to amended Fig. 2; and
Annotated Sheet Showing Changes to amended Fig. 3.



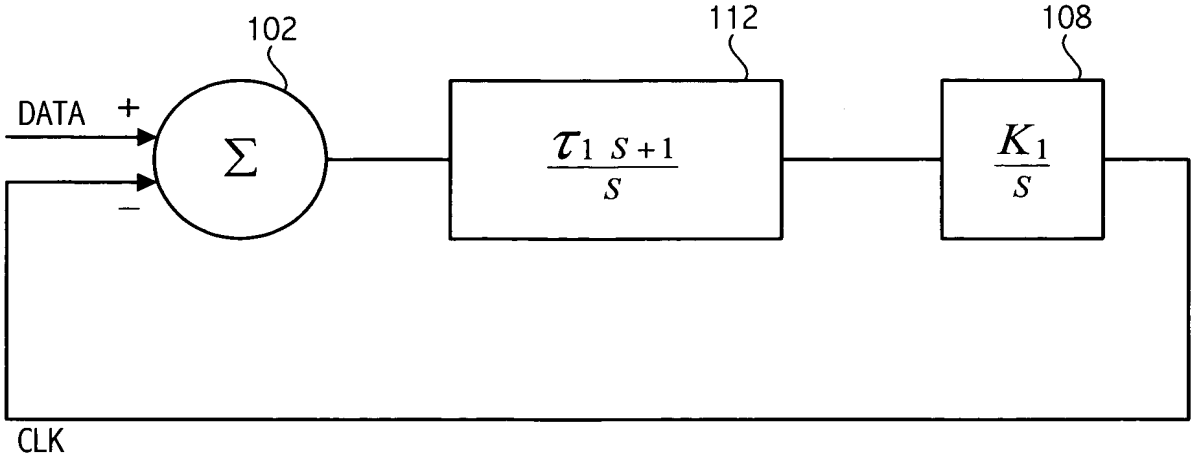
PRIOR ART

FIG. 1A



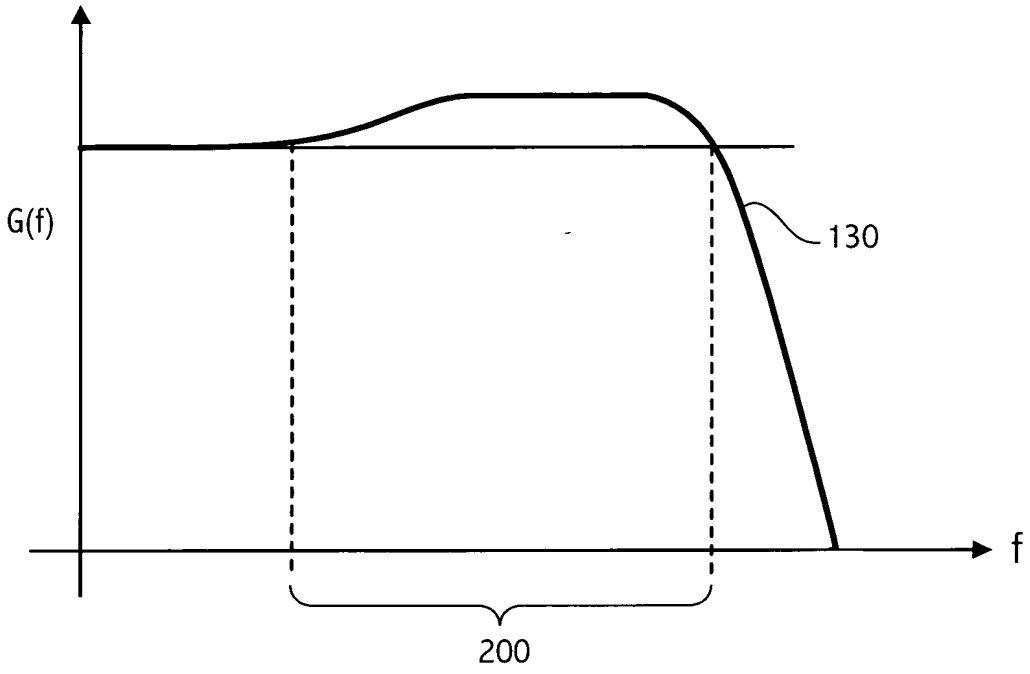
PRIOR ART

FIG. 1B



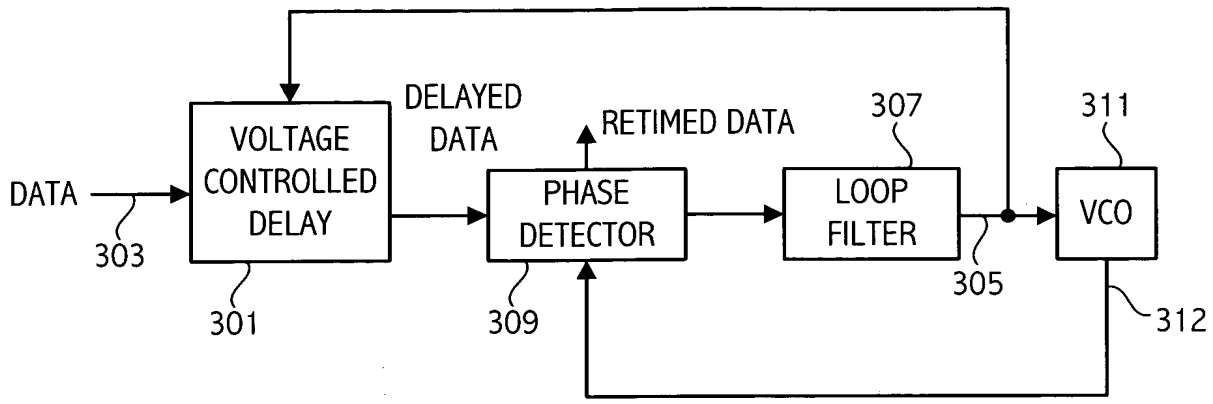
PRIOR ART

FIG. 1C



PRIOR ART

FIG. 2



PRIOR ART

FIG. 3